Customer No.: 31561
Application No.: 10/711,535
Docket No.: 11041-US-PA-1

REMARKS

In The Claims:

1. (currently amended) A method of fabricating a flash memory cell, comprising the following steps:

providing a substrate;

forming a first opening and a second opening in the substrate, wherein the second opening is formed on the bottom of the first opening, the second opening is narrower but is deeper, as measured from the surface of the substrate, than the first opening;

forming a high-voltage doped region under the bottom of the second opening in the substrate;

forming a gate dielectric layer on the substrate in the first opening and the second opening;

forming a conformal conductive layer on the substrate;

performing anisotropic etching to the conformal conductive layer to form ~~forming~~ a first conductive spacer on a sidewall of the first opening as a select gate, and ~~forming~~ a second conductive spacer on a sidewall of the second opening as a floating gate **simultaneously**; and

forming a source region beside the first opening in the substrate.

2. (original) The method of fabricating a flash memory cell of claim 1, wherein the

step of forming the first opening comprises:

forming a mask layer with the pattern of the first opening over the substrate; and

etching the substrate with the mask layer as mask to form the first opening.

3. (original) The method of fabricating a flash memory cell of claim 2, wherein the first opening has round corners on its bottom.

4. (original) The method of fabricating a flash memory cell of claim 2, wherein the step of forming the second opening comprises:

forming spacers on the sidewalls of the mask layer and the first opening; and

etching the substrate, with the mask layer and the spacers as mask, to form the second opening.

5. (original) The method of fabricating a flash memory cell of claim 4, wherein the second opening has round corners on its bottom.

6. (Original) The method of fabricating a flash memory cell of claim 4, wherein the process to form the high-voltage doped region under the bottom of the second opening in the substrate comprises a step of ion implantation, with the mask layer and the spacer as mask, to the substrate.

7. (original) The method of fabricating a flash memory cell of claim 1, wherein the process to form the gate dielectric layer on the surface of the substrate in the first opening and the second opening comprises thermal oxidation.

8. (canceled)

9. (currently amended) The method of fabricating a flash memory cell of claim ~~8~~1, wherein the materials of the conformal conductive layer comprise polysilicon.

10. (original) The method of fabricating a flash memory cell of claim 1, the method further comprises:

forming an insulating layer on the substrate, where the insulating layer covers the select gate and the floating gate; and

forming a contact plug which penetrates through the insulating layer and is electrically connected with the high-voltage doped region.

11. (original) The method of fabricating a flash memory cell of claim 10, the method further comprises a step, before the formation of the insulating layer, to form an insulating spacer on another sidewalls of the select gate and the floating gate so as to protect the floating gate in the process of forming the contact plug.